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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,991	05/02/2001	Jason Seung-Min Kim	NVID-P003124	5788

45594 7590 05/08/2008

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EXAMINER	
MYERS, PAUL R	
ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
05/08/2008	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JASON SEUNG-MIN KIM and ROBERT ALAN BIGNELL

Appeal 2007-2113
Application 09/847,991
Technology Center 2100

Decided: May 8, 2008

Before JOSEPH F. RUGGIERO, ANITA PELLMAN GROSS, and LANCE LEONARD BARRY, *Administrative Patent Judges*.

GROSS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Kim and Bignell (Appellants) appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1 through 27, which are all of the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a cross-bar multipath resource controller including a hardware semaphore unit for permitting each of multiple processors to simultaneously access a different shared resource

while preventing processors from accessing the same resource at the same time. *See generally* Spec. 2:22-4:10. Claim 11 is illustrative of the claimed invention, and it reads as follows:

11. An apparatus for controlling the access to one or more computing resources by one or more processors, the apparatus comprising a resource controller and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources, and wherein the resource controller includes a hardware semaphore unit for controlling access to the one or more resources.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Srini	US 5,053,942	Oct. 01, 1991
Hiller	US 5,081,575	Jan. 14, 1992
Holt	US 5,394,551	Feb. 28, 1995
Dhuey	US 5,805,030	Sep. 08, 1998
Goodwin	US 6,125,429	Sep. 26, 2000
MacLellan	US 6,636,933 B1	Oct. 21, 2003 (filed Dec. 21, 2000)

Claims 1 through 3, 8, 9, 11 through 13, 18, 19, 21, 22, 24, and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Goodwin in view of Holt.

Claims 4 through 7, 10, 14 through 17, 20, 23, and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Goodwin in view of Holt and Hiller.

Claim 27 stands rejected under 35 U.S.C. § 103 as being unpatentable over Goodwin in view of Holt and Dhuey.

Claims 1 through 3, 8, 9, 11 through 13, 18, 19, 21, 22, 24, and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over MacLellan in view of Holt.

Claims 4 through 7, 10, 14 through 17, 20, 23, and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over MacLellan in view of Holt and Hiller.

Claim 27 stands rejected under 35 U.S.C. § 103 as being unpatentable over MacLellan in view of Holt and Dhuey.

Claims 1 through 3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Srini in view of Holt.

Claims 1, 2, 11, 12, 21, and 24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hiller in view of Holt.

Claims 3, 4, 13, 14, 22, 23, 25, and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hiller in view of Holt and Goodwin.

We refer to the Examiner's Answer (mailed October 31, 2006) and to Appellants' Brief (filed September 7, 2006) for the respective arguments.

SUMMARY OF DECISION

As a consequence of our review, we will affirm the obviousness rejections of claims 1 through 3, 8, 9, 11 through 13, 18, 19, 21, 22, 24, and 25 over Goodwin and Holt and over MacLellan and Holt, of claims 4 through 7, 10, 14 through 17, 20, 23, and 26 over Goodwin, Holt, and Hiller and over MacLellan, Holt, and Hiller, and of claim 27 over Goodwin, Holt, and Dhuey and over MacLellan, Holt, and Dhuey. However, we will reverse the obviousness rejections of claims 1 through 3 over Srini and Holt, of

claims 1, 2, 11, 12, 21, and 24 over Hiller and Holt, and of claims 3, 4, 13, 14, 22, 23, and 26 over Hiller, Holt, and Goodwin.

OPINION

Appellants contend (Br. 12) that "Goodwin mentions in passing that an arbiter chip 14 decides which of plural CPUs could have access to data that happened to be in the same memory module," but that "arbiter chip 14 is not the subject of the Goodwin disclosure and is not described or discussed further." Appellants contend (Br. 12) that Goodwin is directed to managing consequences of arbitration and not to access control. Accordingly, Appellants conclude that the "skilled artisan would not have been motivated to combine Goodwin with the other cited art." The first issue, therefore, is whether it would have been obvious in view of the combined teachings of Goodwin and Holt to use a semaphore hardware unit in Goodwin for controlling access to shared resources.

Goodwin discloses (col. 4, ll. 27-51) a crossbar switch connecting multiple CPUs to multiple memory modules, such that each CPU may be connected to a different memory module simultaneously, and an arbiter chip that decides which CPU request for memory has priority for a given memory resource. Thus, Goodwin discloses a mechanism for making sure that only one CPU accesses a memory module at a time. Goodwin does not further discuss the operation of the arbiter chip. However, Holt discloses (col. 1, ll. 14-16) that a semaphore mechanism is used to ensure that only one processing node can access a shared resource at a time.

The Supreme Court has held that in analyzing the obviousness of combining elements, a court need not find specific teachings, but rather may

consider "the background knowledge possessed by a person having ordinary skill in the art" and "the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-41 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id* at 1740.

In the present case, Goodwin suggests the need to ensure only one CPU has access to a given memory at a time, but does not disclose the details of the arbiter chip that performs that function. Holt discloses that a hardware semaphore can be used to perform the aforementioned function. The use of a hardware semaphore in Goodwin would have been no more than the predictable use of a semaphore according to its established function, and, therefore, would have been an obvious improvement. Accordingly, we will sustain the obviousness rejection of claims 1 through 3, 8, 9, 11 through 13, 18, 19, 21, 22, 24, and 25 over Goodwin in view of Holt.

Regarding the rejection of claims 4 through 7, 10, 14 through 17, 20, 23, and 26 over Goodwin in view of Holt and Hiller and of claim 27 over Goodwin in view of Holt and Dhuey, Appellants have presented no arguments regarding the addition of either Hiller or Dhuey to the primary combination. Therefore, we will sustain the obviousness rejections of claims 4 through 7, 10, 14 through 17, 20, 23, 26, and 27 for the same reasons as stated *supra*.

Appellants contend (Br. 6-9) that the Examiner erred in relying upon MacLellan's message network 260 to satisfy the claimed resource controller. The Examiner (Ans. 15) admits that the wrong item was previously identified as satisfying the controller. The Examiner (Ans. 7) points to

crossbar switch system interface 160 as performing the functions for the resource controller recited in the claims. Specifically, the Examiner (Ans. 7 and 15) asserts that the switch allows one or more processors within 120 to access one or more memory resources within memory 220 simultaneously. Further, Appellants contend (Br. 9) that MacLellan "describes an asynchronous system in which simultaneous access of disk drives by processors is neither possible nor necessary." However, the Examiner (Ans. 15) points to portions of columns 14 and 18 of MacLellan as disclosing plural processors simultaneously accessing different resources. The next issue, therefore, is whether MacLellan discloses multiple processors each simultaneously accessing a different resource.

MacLellan discloses (col. 5, ll. 58-63) that each front end director 180 includes a microprocessor 299 (or CPU) and that the microprocessor makes a request for data from global cache memory 220. Figure 8 shows several front end director boards cross-connected to several memory boards of cache memory 220. MacLellan discloses (col. 14, ll. 36-38, and col. 18, ll. 50-53, both cited by the Examiner in the Answer) that crossbar switches 5004 process *parallel* information, and that *simultaneous* transfers occur. Thus, we agree with the Examiner's position in the Answer that MacLellan discloses plural processors each simultaneously accessing a different resource. Appellants' argument on page 9 of the Brief that MacLellan describes an asynchronous system and that simultaneous access is not possible do not explain why the portions regarding parallel processing and simultaneous transfer, noted *supra* and relied upon by the Examiner, do not disclose simultaneous access. Further, since the remaining arguments, which are directed to element 260, are moot in view of the Examiner's

correction in the Answer, and since Appellants did not respond to the correction by submitting a Reply Brief, we have no arguments from Appellants to convince us of error on the part of the Examiner regarding the use of MacLellan.

Appellants (Br. 9-10) contend that MacLellan fails to teach semaphores for controlling access to shared resources. However, the Examiner applied the teachings of Holt for a suggestion to use semaphores. Accordingly, we will sustain the obviousness rejection of claims 1 through 3, 8, 9, 11 through 13, 18, 19, 21, 22, 24, and 25 over MacLellan in view of Holt. In addition, since Appellants provided no arguments regarding the additional reference of Hiller or Dhuey, we will sustain the rejection of claims 4 through 7, 10, 14 through 17, 20, 23, and 26 over MacLellan in view of Holt and Hiller and of claim 27 over MacLellan in view of Holt and Dhuey for the same reasons explained *supra*.

As to the rejection of claims 1 through 3 over Srini in view of Holt, Appellants contend (Br. 10-11) that Srini's disclosure of a fairness-based arbitration scheme that forces alternation of access rights each cycle is incompatible with a semaphore-based arbitration which permits using a resource until the operation is completed. The Examiner asserts (Ans. 17) that it would have been obvious to use a semaphore to control access when the memory is busy. The issue is whether Srini is incompatible with the use of semaphores.

We agree with Appellants that Srini's forced alternation of access rights is contrary to a semaphore-based arbitration. Although Srini discloses (col. 4, ll. 34-36) that arbiters prevent processors from simultaneously being connected to a particular memory at a time, the arbiters work differently

from semaphores. Therefore, it would not have been obvious to substitute semaphores for the arbiters. Thus, we cannot sustain the obviousness rejection of claims 1 through 3.

Regarding the rejection of claims 1, 2, 11, 12, 21, and 24 over Hiller in view of Holt, Appellants contend (Br. 13) that Hiller teaches eliminating the need for arbitration and, therefore, "obviates the use of semaphore controlled access to shared resources because contention is eliminated." The Examiner admits (Ans. 19) that Hiller eliminates the need for arbitration, but still maintains that it would have been obvious to include a semaphore. This last issue is whether it would have been obvious in view of the teachings of Hiller and Holt to include a semaphore in Hiller.

Hiller discloses (abstract) "a parallel processing system free of memory conflicts." Hiller further discloses (col. 7, ll. 3-6) that predetermining the crossbar switch configuration when the PE microcode algorithms are developed "eliminates the need for arbitration of access to PMEM's during run time." Thus, Hiller clearly teaches away from including a semaphore, the purpose of which is to ensure that only one processor has access to a given resource at a time. Consequently, the combination of Hiller and Holt would not have been obvious, and we cannot sustain the obviousness rejection of claims 1, 2, 11, 12, 21, and 24.

For claims 3, 4, 13, 14, 22, 23, 25, and 26, the Examiner adds Goodwin to the combination of Hiller and Holt. However, Goodwin does not cure the deficiency of the primary combination of Hiller and Holt. Therefore, we cannot sustain the obviousness rejection of claims 3, 4, 13, 14, 22, 23, 25, and 26.

ORDER

We have sustained the rejections of claims 1 through 3, 8, 9, 11 through 13, 18, 19, 21, 22, 24, and 25 both over Goodwin in view of Holt and also over MacLellan in view of Holt. We likewise have sustained the rejections of claims 4 through 7, 10, 14 through 17, 20, 23, and 26 both over Goodwin in view of Holt and Hiller and also over MacLellan in view of Holt and Hiller. We have further sustained the rejections of claim 27 both over Goodwin in view of Holt and Dhuey and also over MacLellan in view of Holt and Dhuey. On the other hand, we have reversed the rejections of claims 1 through 3 over Srini in view of Holt, of claims 1, 2, 11, 12, 21, and 24 over Hiller in view of Holt, and of claims 3, 4, 13, 14, 22, 23, 25, and 26 over Hiller in view of Holt and Goodwin. As we have sustained at least one rejection for each claim, the decision of the Examiner rejecting claims 1 through 27 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

gvw

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